While no claims have been amended herein, certain claims are set forth below in *unamended* form for the convenience of the Examiner. Note: new claims have been added.

1. (*Unamended*) A thin-film transistor comprising

a semiconductor layer and multiple gate electrodes that have been formed over the semiconductor layer, wherein the semiconductor layer includes:

first and second heavily doped regions, which have a first conductivity type, are spaced apart from each other and serve as source/drain regions;

a plurality of channel regions, which have a second conductivity type, are located between the first and second heavily doped regions so as to face the gate electrodes, and include first and second channel regions, wherein the first channel region is closer to the first heavily doped region than any other one of the channel regions is, while the second channel region is closer to the second heavily doped region than any other one of the channel regions is;

an intermediate region, which has the first conductivity type and is located between two mutually adjacent ones of the channel regions;

a first lightly doped region, which has the first conductivity type and is located between the first channel region and the first heavily doped region;

a second lightly doped region, which has the first conductivity type and is located between the second channel region and the second heavily doped region;

a third lightly doped region, which has the first conductivity type, has a carrier concentration different from that of the first lightly doped region and is located between the first lightly doped region and the first channel region; and

a fourth lightly doped region, which has the first conductivity type, has a carrier concentration different from that of the second lightly doped region and is located between the second lightly doped region and the second channel region.

14. (*Unamended*) A thin-film transistor comprising:

a semiconductor layer and multiple gate electrodes that have been formed over the semiconductor layer,

wherein the semiconductor layer includes:

first and second heavily doped regions, which are spaced apart from each other and serve as source/drain regions;

a plurality of channel regions, which are located between the first and second heavily doped regions so as to face the gate electrodes and which include first and second channel regions, wherein the first channel region is closer to the first heavily doped region than any other one of the channel regions is, while the second channel region is closer to the second heavily doped region than any other one of the channel regions is;

an intermediate region located between two mutually adjacent ones of the channel regions;

a first lightly doped region located between the first channel region and the first heavily doped region; and

a second lightly doped region located between the second channel region and the second heavily doped region, and

wherein the first channel region includes a first intrinsic channel region and the second channel region includes a second intrinsic channel region.

16. (*Unamended*) The transistor of claim 14, wherein the first channel region includes a doped channel region between the first intrinsic channel region and the intermediate region, while the second channel region includes a doped channel region between the second intrinsic channel region and the intermediate region.

Please add the following new claims:

25. (*New*) The thin-film transistor of claim 1, wherein the carrier concentration of the first lightly doped region is substantially higher than that of the third lightly doped region, the first and third lightly doped regions being located immediately adjacent one another.

26. (*New*) The thin-film transistor of claim 25, wherein the carrier concentration of the second lightly doped region is substantially higher than that of the fourth lightly doped region, the second and fourth lightly doped regions being located immediately adjacent one another.

27. (*New*) A thin-film transistor including a semiconductor layer, multiple gate electrodes formed over the semiconductor layer, and wherein the semiconductor layer comprises:

first and second heavily doped regions spaced apart from each other that serve as source/drain regions;

at least first and second spaced apart channel regions located between the first and second heavily doped regions under respective gate electrodes; and

first and second immediately adjacent lightly doped regions located between the first channel region and the first heavily doped region, wherein the first lightly doped region is located closer to the first channel region than is the second lightly doped region, and wherein the first lightly doped region has a carrier concentration less than that of the second lightly doped region which is closer to the first heavily doped region.

REMARKS

This is in response to the Office Action dated May 7, 2003. Non-elected claims 11-13 and 21-22 have been canceled, without prejudice in view of the Restriction Requirement. New claims 25-27 have been added. Thus, claims 1-10, 14-20 and 23-27 are now pending. While claims 23-24 have been withdrawn from consideration, they are dependent claims. Thus, claims 23-24 will properly be in condition for allowance once the claims from which they depend are allowed.